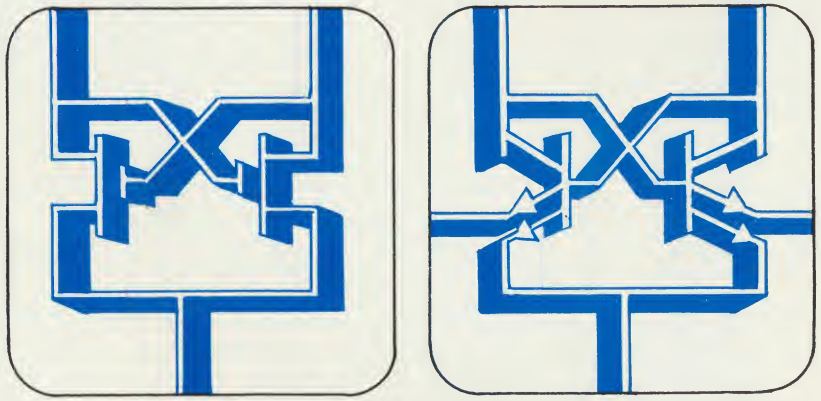
AN INTENSIVE TWO-DAY COURSE FOR SENIOR ENGINEERS ON "APPLICATION OF SEMICONDUCTOR MEMORIES"



FEATURING PRACTICAL UP-TO-DATE APPLICATION TECHNIQUES

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APPLYING SEMICONDUCTOR MEMORIES.

MARCIAN E. HOFF. Manager, Applications Research. Intel Corporation.

Costs of semiconductor memories are rapidly becoming competitive with ferrite cores, and may soon replace cores in many applications. An intermix of MOS shift registers and MOS dynamic-refresh memory may behave much like a high-performance drum/core combination. While semiconductor components may initially act as substitutes for corresponding magnetic memory components, higher performance may also be achieved by reorganizing computer architecture to take advantage of such features as parallel access and modularity. New means for implementing higher level languages may be necessary to fully use the performance these memories can achieve.

MOS READ-ONLY MEMORIES.

MICHAEL R. McCOY. Manager, Advanced Product Development. Electronic Arrays, Inc.

The past few years have seen a number of painful, sometimes abortive, attempts by MOS manufacturers to introduce large scale read-only memories. However, the MOS read-only memory has now arrived and is ready for acceptance. Applications of MOS read-only memories are numerous with new uses rapidly being discovered. Character generators use read-only memories to convert the digital character code to a screen code for dot matrix characters. Another exciting application is the fixed storage for a microprogrammed digital processor. All forms of code converters are prime candidates for implementation as read-only memories.

MOS ICs AND MEMORY PROGRAM APPLICATIONS.

E. FLOYD KVAMME. Microcircuits Product Manager. National Semiconductor Corporation.

Presently available read-only memories can in general be used to finalize conversion systems in that the read-only memory can be used as a micro-programmer which utilizes the proper logic conditions at the input of a data processor. A simple arithmetic unit will be shown which illustrates this use of read-only memories. In addition, the applications of read-only memories will be discussed.

A COMPARISON OF TTL, CML AND MOS/BIPOLAR MEMORY CIRCUIT TECHNIQUES.

ANDREW R. BERDING, Vice President, Engineering. Advanced Memory Systems, Inc.

Designing an integrated random access memory (RAM) involves choosing a circuit technology. The possibilities are (1) Transistor-transistor logic techniques with and without anti-saturation clamps for all memory functions, (2) Current mode techniques for all memory functions including storage, (3) Mixed TTL/CML approaches using both philosophies to capture some advantages from each, (4) MOS-Bipolar hybrids employing bipolar support and MOS storage chips.

APPLICATION OF ION-IMPLANTED READ-ONLY MEMORIES CIRCUITS.

CARROLL PERKINS. Manager, Applications. Hughes Aircraft.

The use of ion-implanted techniques allows the building of read-only memories with less than 300-ns access times. A 2048-bit ion-implanted memory with this speed capability is currently in prototype production. It's use will be described. Also to be covered will be a comparison of ion-implanted memories with standard p-channel MOS structures.

HIGH-SPEED RANDOM-ACCESS MEMORIES.

BUD BROEKER. Applications Engineer. Motorola Semiconductor.

High-speed random access memories can be built using bipolar and bipolar/MOS hybrid combinations. Recently developed emitter-coupled-logic bipolar devices are increasing the speed capabilities obtainable from semiconductor memories. The use of an 8000-bit hybrid/ECL memory stack will be described along with interfacing requirements for expansion into larger systems.

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Two key problems now facing equipment/system designers are (1) determining which semiconductor devices are best suited for their applications, and (2) designing to take maximum advantage of the capabilities of these devices.

These problems are currently of particular concern to engineers planning to use or designing with semiconductor memories. Today, engineers have a number of competing approaches available to them to choose from such as metal-oxide-semiconductor (MOS), bipolar TTL, current mode, MOS/bipolar hybrid, silicon-gate MOS, etc. There is considerable disagreement on the organization of memories and what should go on the chip. The services and policies of suppliers concerning customizing vary widely. To shed some light on the various ways to design with semiconductor memories and to pass along important up-to-date design rules and techniques, EEE has organized an intensive two-day course/seminar on the "Application of Semiconductor Memories." The speakers are fifteen leading specialists at semiconductor-memory companies. Each one is directly concerned with the application of his company's memories by customers and therefore is uniquely qualified to participate in this course.

FEATURING PRACTICAL UP-TO-DATE APPLICATION TECHNIQUES

CONVERTING FROM BINARY TO BCD DECIMAL NUMBERS WITH READ-ONLY MEMORIES AND ADDERS.

ED TARBOX. Manager, IC Applications and Evaluation. Sylvania Semiconductor.

A technique for converting binary numbers to binary coded decimal numbers using bipolar read-only memories will be described. The ROM's decode the binary number in sets which are then summed to produce the BCD value of the binary number. Clock or shift pulses are not required and conversion speeds of 180-ns are typical for a 13-bit binary number.

RANDOM-ACCESS MEMORY APPROACHES.

JERRY LUECKE. Applications Engineer. Texas Instruments.

Various types of memories, memory cells of various characteristics and alternate decoding methods are available to achieve a particular memory speed. Each has specific advantages and disadvantages which will be discussed.

APPLICATIONS FOR RANDOM-ACCESS BIPOLAR MEMORIES.

MELVIN G. SNYDER, Planning Manager, Raytheon Company.

Currently, the basic building block used in designing large bipolar semiconductor memories is the 64-bit random-access memory (organized 16 words by 4-bits). From this memory, the requirements for varying word sizes and bit lengths of scratchpad and cache (buffer) memories are being met. Designers of these and mainframe memories, planning to incorporate bipolar semiconductor RAMs, have many factors to weigh. Packaging considerations and economics are involved in the decision as to which design route to take.

DESIGNING YOUR OWN MOS MEMORIES.

ROBERT NORMAN. President. Nortec Electronics Corporation.

It's possible today for an engineer to conduct part of the design cycle for an MOS IC at his own facility and then farm out the rest of the job to a supplier. How much of the work the engineer should do himself and how much should be subcontracted requires careful evaluation of the economics involved.

MOS AND BIPOLAR MEMORIES WITH DIELECTRIC ISOLATION.

DAVE UIMARI. Application Engineer. Radiation Inc.

Recently, both programmable bipolar memories and complementary-symmetry MOS memories have become commercially available. The programmable bipolar memory permits the IC user to take an unprogrammed memory off the shelf and using a power supply instantly convert it to a permanent programmed memory. The appilcation of a programmable 512-bit 64-word 8-bits-per-word TTL memory and a complementary-symmetry 200-ns MOS random-access memory with 256 bits (32 words 8 bits per word organization) will be described.

APPLICATION CONSIDERATIONS FOR MTNS (Metal-Thick oxide-Nitride-Semiconductor) LSI.

JULES HERTSCH, Applications Manager. General Instrument.

The use of nitride in building large-scale intergrated circuits has changed some of the rules for system design engineers. This talk investigates the use of nitride-processed ICs in several applications.

A VERSATILE LOW-COST MOS READ-WRITE RAM.

JOSEPH H. FRIEDRICH. Supervisor, MOS Memory Product Development. Philco-Ford.

Now that read-write semiconductor memories are available, the system designer has much more flexibility in building the memory sections of his equipment and systems. To illustrate the various possibilities available to the design engineer in creating memory systems, the application of a 256-word by 1-bit-per-word memory will be explored. This memory uses enhancement-mode transistors exclusively. Interface and cost considerations for both the chip and the memory system will be covered.

MEGABIT HIGH-SPEED BIPOLAR MEMORIES.

DR. WENDELL SANDERS. Head, Memory Systems Engineering, R & D. Fairchild Semiconductor.

High-speed bipolar memory systems can be designed using a modular approach. The techniques and procedures used for the 131072-bit memory system of the Illiac IV computer system will be described.

RELIABILITY AND COST CONSIDERATIONS FOR HYBIRD RANDOM-ACCESS MEMORIES.

ANTHONY HOLBROOK. Manager, IC Design. Computer Microtechnology.

The design of memory systems using bipolar ICs for decoding driving and sensing and MOS ICs for storage can lead to an optimum cost/performance design. Other considerations which can also lead to optimum cost/performance designs include a single metal system for beams on the IC chips in a double-layer metalized substrate system.

CONDUCTOR MEMORIES"

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TIME AND PLACE — This two-day course on "Application of Semiconductor Memories For Senior Engineers" will be held Wednesday-Thursday, May 6-7, 9:00 AM to 5:00 PM (during Spring Joint Computer Conference week) at The Traymore, Boardwalk at Illinois Avenue, Atlantic City, New Jersey.

REGISTRATION FEE — The $155 fee includes registration, related course materials, luncheons, coffee breaks, and a mahogany-plaqued certificate of course completion.

TAX DEDUCTION OF EXPENSES — An income tax deduction is allowed for expenses of education (including travel, meals and lodging) undertaken to maintain and improve professional skills (see Treas. Reg. 1.162.5; Coughlin vs. Commissioner, 203 F. 2d 307).

TICKETS — Confirmed registrations cancelled later than two weeks before the meeting are subject to a $25 service charge. Registrants whose applications have been confirmed and who fail to attend a meeting are liable for the entire fee unless they contact the Registrar prior to the meeting to cancel their reservations.

HOTEL ACCOMMODATIONS — Your hotel accommodation is not included in the registration fee. It is rcommended that you make reservations as early as possible. Please arrange room accommodations directly with The Traymore or the hotel of your choice. However, should you have any problem, EEE's Seminar Registrar can assist you.

HOW TO REGISTER — Fill out the form and return to EEE in advance of the seminar. If more convenient, you may phone the Registrar at 212-661-0450. All applications must be confirmed and applicants should not come to the seminar without confirmation. EEE reserves the right to limit enrollment.

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